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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,020	03/31/2004	Yen Sheng Chang	BHT-3244-41	3877

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TROXELL LAW OFFICE PLLC
SUITE 1404
5205 LEESBURG PIKE
FALLS CHUCH, VA 22041

EXAMINER	
BONURA, TIMOTHY M	
ART UNIT	PAPER NUMBER
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,020	CHANG, YEN SHENG	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10 and 11* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

- **Claims 1-7, and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Poisner, U.S. Patent Number 6,535,988.**

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Poisner, U.S. Patent Number 6,535,988.

3. Regarding claim 1:

a. Regarding the limitation of "setting a clock, applied in a clock generating device of a computer motherboard and setting the clock according to a signal status of a basic input/output system (BIOS)," Poisner discloses a system with a system processor clock and a real-time, fixed stable clock, (Lines 12-17 of Column 4) and detecting an irregular system clock status (Lines 40-45 of Column 4).

b. Regarding the limitation of "detecting if a signal output from the BIOS is irregular," Poisner discloses a system with detecting an over-clock in a system processor. (Lines 12-15 of Column 4).

c. Regarding the limitation of "replacing an original setting value of a memory inside a logic control unit by a frequency setting value pre-stored in a memory unit if the signal output from the BIOS is irregular," Poisner discloses a system with a stable fix clock for

compare a system clock with a fixed, stable, real-time clock signal and disabling the irregular processor clock. (Lines 47-55 of Column 4).

d. Regarding the limitation of "finishing an auto-booting process," Poisner discloses a system wherein BIOS reads the status signals and refers the user to service the computer upon booting the computer. (Liens 60-65 of Column 8).

4. Regarding claim 2:

e. Regarding the limitation of "setting a clock, applied in a clock generating device of a computer motherboard and setting the clock according to a trigger signal," Poisner discloses a system with a system processor clock and a real-time, fixed stable clock, (Lines 12-17 of Column 4) and detecting an irregular system clock status (Lines 40-45 of Column 4).

f. Regarding the limitation of "detecting if the trigger signal is input," Poisner discloses a system with detecting an over-clock in a system processor. (Lines 12-15 of Column 4).

g. Regarding the limitation of "replacing an original setting value of a memory inside a logic control unit by a frequency setting value pre-stored in a memory unit if the trigger signal is input," Poisner discloses a system with a stable fix clock for compare a system clock with a fixed, stable, real-time clock signal and disabling the irregular processor clock. (Lines 47-55 of Column 4).

h. Regarding the limitation of "finishing an auto-booting process," Poisner discloses a system wherein BIOS reads the status signals and refers the user to service the computer upon booting the computer. (Liens 60-65 of Column 8).

5. Regarding claim 3, Poisner discloses a system with a thermal management to detect an over-heating of the processor to indicate an over-clocking situation. (Lines 12-20 of Column 7).

6. Regarding claim 4:

i. Regarding the limitation of "a crystal oscillator," Poisner discloses a system with a crystal oscillator. (Lines 62-67 of Column 4).

j. Regarding the limitation of "a frequency control unit," Poisner discloses a system with a frequency being set a fixed setting. (Lines 62-67 of Column 4).

k. Regarding the limitation of "a PLL spread-spectrum unit electrically connected with the crystal oscillator and the frequency control unit," Poisner discloses a system with a crystal oscillator connected to a PLL for frequency setting. (Lines 6-15 of Column 6).

l. Regarding the limitation of "a memory unit having a clock setting value stored therein," Poisner discloses a system with a system processor clock and a real-time, fixed stable clock, (Lines 12-17 of Column 4) and detecting an irregular system clock status (Lines 40-45 of Column 4).

m. Regarding the limitation of "a detection control unit electrically connected with the memory unit and used to detect a signal status," Poisner discloses a system with detecting an over-clock in a system processor. (Lines 12-15 of Column 4).

n. Regarding the limitation of "a logic control unit electrically connected with the PLL spread-spectrum unit, the frequency control unit and detection control unit," Poisner discloses a system with a stable fix clock for compare a system clock with a fixed, stable, real-time clock signal and disabling the irregular processor clock. (Lines 47-55 of Column 4).

7. Regarding claim 5, Poisner discloses a system that uses BIOS stored on memory firmware. (Lines 24-27 of Column 4). It is inherent the firmware can be EEPROM.

8. Regarding claim 6, Poisner discloses a system with detecting an over-clock in a system processor. (Lines 12-15 of Column 4).

9. Regarding claim 7, Poisner discloses a system with detecting an over-clock in a system processor. (Lines 12-15 of Column 4).

10. Regarding claim 10, Poisner discloses a system wherein the BIOS stores proper system clock settings. (Lines 1-5 of Column 4).

11. Regarding claim 11, Poisner discloses a system wherein the BIOS stores proper system clock settings. (Lines 1-5 of Column 4).

Allowable Subject Matter

12. Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

14. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman.**

- The supervisor can be reached on **571-272-3644.**

15. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

17. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100.**

18. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

  Alexandria, VA 22313-1450

Tim Bonura
Examiner
Art Unit 2114

January 6, 2007